

C L A I M S

1. An display apparatus, for conducting video display through address operation on display lines upon basis of a video signal, wherein:

5 scanning pulses of same phase are applied to plurality of first display lines in a first field, building up a one frame therewith, and scanning pulses of same phase are applied to plurality of second display lines in a second field thereof, thereby conducting the address operation.

10 2. An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein:

15 scanning pulses of same phase are applied to the X electrodes of first display lines in a first field, building up a one frame therewith, and scanning pulses of same phase are applied to the Y electrode of second display lines in a second field thereof, thereby conducting the address operation, so as to perform video  
20 display thereon.

25 3. An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein:

scanning pulses of same phase are applied to plural numbers of first display lines, neighboring to each other on a first field, building up a one field therewith, and scanning pulses of same phase are applied to plural numbers of second display lines,

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neighboring to each other on a second field thereof, thereby conducting the address operation, so as to perform video display thereon.

4. An display apparatus, comprising: X and Y electrodes, being disposed in parallel to each other in a pair, for forming one display line therewith, and an address electrode being disposed to separate from and to cross over said both electrodes, in plural numbers thereof, wherein:

said X and Y electrodes are disposed in reversed in the order thereof on display lines neighboring to each other;

scanning pulses of same phase are applied to the X electrodes of plural number of first display lines, neighboring to each other on a first field, building up a one field therewith, and scanning pulses of same phase are applied to the Y electrodes of plural numbers of second display lines, neighboring to each other on a second field thereof, thereby conducting the address operation, so as to perform video display thereon.

5. An display apparatus, as defined in the claim 1, claim 2, claim 3, or claim 4, wherein voltage values of the address pulses applied to said first field and said second field.

6. An display apparatus, comprising parallel display electrodes  $X(i)$  ( $i=1$  through  $n$  ( $n$ : a positive number), an electrode of  $i^{\text{th}}$  number), and address electrodes  $A(j)$  ( $j=1$  through  $k$  ( $k$ : a positive number), an electrode of  $j^{\text{th}}$  number), being separated and crossing over said display electrodes  $X(i)$ , wherein:

conducting light emission display on the display electrodes  $X(4p+1)$  and  $X(4p+2)$  ( $p$ : a positive number including zero (0)), in a first period of a first field;

conducting light emission display on the display electrodes

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X(4p+3) and X(4p+4), in a second period of the first field;

conducting light emission display on the display electrodes X(4p+2) and X(4p+4), in a third period of a second field; and

conducting light emission display on the display electrodes X(4p+4) and X(4p+5), in a fourth period of the second field.

7. An display apparatus, as defined in the claim 6, wherein the said first, second, third and fourth periods are divided into plural numbers of sub-fields, respectively, and said sub-field includes an address period for applying a scanning pulse to at least one display electrode of a pair of the display electrodes X, so as to conduct write-in discharge depending upon video information between the address electrodes A, and a display period for sustaining discharge by means of wall electric charge developed in said address period.

8. An display apparatus, as defined in the claim 7, wherein alignment orders of the plural numbers of sub-fields formed within said first, second, third and fourth periods are different in at least one of said first, second, third and fourth periods.

9. An display apparatus, as defined in the claim 7, wherein a full write-in pulse, for making all discharge cells to conduct the write-in discharge, is applied onto one of the display electrodes X forming said pair, in advance to a period during when the write-in discharge is conducted in at least one sub-field of said plural numbers of sub-fields, while a voltage pulse of causing no full write-in discharge is applied at least one of those of the display electrodes X other than the above.

10. An display apparatus, as defined in the claim 7, wherein at least two (2) of the display electrodes to be applied with said scanning pulses thereon are connected in common, and the display electrodes neighboring with said display electrode are driven with

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outputs having different waveforms.

11. An display apparatus, comprising parallel display electrodes  $X(i)$  ( $i=1$  through  $n$  ( $n$ : a positive number), an electrode of  $i^{\text{th}}$  number), and address electrodes  $A(j)$  ( $j = 1$  through  $k$  ( $k$ : a positive number), an electrode of  $j^{\text{th}}$  number), separately crossing over said display electrodes  $X(i)$ , wherein:

forming a pair with the display electrodes  $X(3p+1)$  and  $X(3p+2)$  ( $p$ : a positive number including zero (0)), and conducting light emission display on the display electrodes of said pair, in a first period of a field;

forming a pair with the display electrodes  $X(3p+2)$  and  $X(3p+3)$  and conducting light emission display on the display electrodes of said pair, in a second period of the field; and

forming a pair with the display electrodes  $X(3p+3)$  and  $X(3p+4)$  and conducting light emission display on the display electrodes of said pair, in a third period of the field.

12. A display apparatus, constructing a display screen by disposing discharge cells in a matrix-like manner, each discharge cell being constructed with a pair of display electrodes being parallel to each other and covered with a dielectric body, and with a set of an address electrode being disposed in a direction of crossing thereover, wherein:

address electrodes are disposed in common for a first panel portion and a second panel portion, constructing said display screen therewith;

operating address operation, sequentially, all said discharge cells of said first panel portion, by scanning one of the pair of display electrodes of said first panel portion, sequentially, while applying a selection pulse between the display

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electrode and an address electrode, and applying an alternating sustain pulse onto all said pair of display electrodes of said first panel portion of said discharge cells being operated by the address operation, simultaneously, thereby conducting display sustain operation; and

operating address operation, sequentially, all said discharge cells of said second panel portion, by scanning one of the pair of display electrodes of said second panel portion, sequentially, while applying a selection pulse between the display electrode and an address electrode, and applying an alternating sustain pulse onto all said pair of display electrodes of said second panel portion of said discharge cells being operated by the address operation, simultaneously, thereby conducting display sustain operation; and further having:

a time band, during which the address operation of said first panel portion and the display sustain operation of said second panel portion coincide with each other.

13. A display apparatus, as defined in the claim 12, further comprising a reset period for applying a pulse for address preparation prior to said address operations of said first and second panel portions, and a blanking period for interrupting the address operation on said first panel portion at same time of the reset period of said second panel portion.

14. A display apparatus, as defined in the claim 13, wherein the scanning of the display electrodes of one of said first and second panel portions is conducted, sequentially, in a direction of approaching to a boundary between said first and second panel portions, and time when conducting the scanning in vicinity of said boundary of said first panel portion is after completion of the reset period of said second panel portion.

15. A display apparatus, as defined in the claim 12, wherein

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the scanning on said first and second panel portions is conducted, by conducting same display on two (2) lines with application of the scanning pulses of same time to one of the display electrodes of each of two of said pairs of the display electrodes neighboring with each other, in a first field, while conducting same display on two (2) lines with application of the scanning pulses of same time to one of the display electrodes of each of two of said pairs of a combination differing from the two of said pairs of display electrodes neighboring with each other, in a second field.

16. A display apparatus, as defined in the claim 12, wherein a rib is formed on a border between said first panel portion and said second panel portion, for cutting off movement of discharging electric charge caused between said discharge cells of said first and second panel portions in vicinity of said boundary.

17. A display apparatus, as defined in the claim 12, wherein voltage transition period of the alternating sustain pulses, which are to be applied to the pair of electrodes by the display sustain operation of said second panel portion, is included within a voltage hold period of the address pulse to be applied to said address electrode by the address operation of said first panel portion.

18. A display apparatus, having at least plural numbers of parallel scan electrodes and plural numbers of parallel address electrodes crossing over said scan electrodes separately, wherein discharge cells are formed at intersection points of said scanning electrodes and said address electrodes, and said discharge cells are disposed in a matrix-like manner, wherein:

applying scanning pulse to said scanning electrode for conducting line selection, applying address pulse depending upon information onto said address electrode, and applying voltage for sustaining said address discharge after completion of application of said scanning pulse, onto the scan electrode just after completion of said scanning pulse, in the address operation for

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conducting write-in by causing the address discharge which is caused by said scanning pulse and said address pulse.

19. A display apparatus, as defined in the claim 18, wherein the voltage for sustaining said address discharge has a voltage value of causing no discharge between said scan electrodes and said address electrode by voltage of said address pulse together with.

20. A display apparatus for performing video display on display lines by operating address operation upon basis of a signal, wherein:

operating an address operation on plural numbers of first display lines upon basis of a same information, in a first field constructing one (1) frame, and operating an address operation on plural numbers of second display lines upon basis of the same information, in a second field thereof.

21. A video display method for performing video display on display lines by operating address operation upon basis of a signal, wherein:

after applying a scanning pulses of same phase onto plural numbers of first display lines upon basis of a same information, in a first field constructing one (1) frame, then, address operation is conducted by applying the scanning pulses of same phase onto plural numbers of second display lines in a second field thereof.

22. A video display method for performing video display on display lines by operating address operation based on a signal, wherein:

after operating an address operation on plural numbers of first display lines with same information, in a first field constructing one (1) frame, then, operating the address operation

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on plural numbers of second display lines with the same information, in a second field thereof.

23. A video display method for performing video display by using plural numbers of display lines, wherein:

5       the video display is performed by dispersing said plural numbers of display lines on plural numbers of time bands obtained from one (1) frame by dividing it into three (3) or more.

24. A video display apparatus, comprising a panel portion, which has plural numbers of elements, each including display electrodes forming a pair and constructing a display line and an address electrodes which crosses over said display electrodes, wherein:

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an address electrode is provided being connected in common to a first panel portion and a second panel portion, and an address period of a sub-field in said first panel portion and a display period of a sub-field in said second panel portion overlap with each other.

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25. A video display apparatus, comprising a panel portion, which has plural numbers of elements, each including display electrodes forming a pair and constructing first and second display lines and an address electrodes which crosses over said display electrodes, comprising:

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means for conducting same address operation by applying scanning pulses of same phase to said first display line of plural number of display lines, and a driver portion for driving plural numbers of display electrodes with driving pulses differing from each other.

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26. A video display apparatus, as defined in the claim 25, wherein said driving pulses are different in phases thereof between

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said second display electrodes.

27. A video display apparatus, as defined in any one of the claims 1 through 20, and 24 through 26, wherein said video display apparatus is a plasma display apparatus.

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Fig. 1 Scan IC Scan IC Sustain Driver Scan IC Scan IC  
Scan IC Sustain Driver

Fig. 2

Fig. 3 Scan IC Scan IC Scan IC Scan IC Sustain Driver  
5 Sustain Driver

Fig. 4 Fig. 5 Fig. 6

First Field Second Field 1<sup>st</sup> Line 2<sup>nd</sup> Line 3<sup>rd</sup> Line 4<sup>th</sup> Line  
5<sup>th</sup> line 6<sup>th</sup> line 7<sup>th</sup> line

Fig. 7 XY/XY Type XY/YX type

10 Fig. 8 First Field Second Field

Fig. 9 Scan IC Scan IC Scan IC Sustain Driver  
Sustain Driver Scan IC Scan IC

Fig. 10 Scan IC Scan IC Scan IC Scan IC Scan IC Scan IC  
Sustain Driver Sustain Driver

15 Fig. 11 First Field Second Field

Fig. 12 1<sup>st</sup> Period of 1<sup>st</sup> Field 2<sup>nd</sup> Period of 1<sup>st</sup> Field  
3<sup>rd</sup> Period of 2<sup>nd</sup> Field 4<sup>th</sup> Period of 2<sup>nd</sup> Field  
1<sup>st</sup> Phase 2<sup>nd</sup> Phase 3<sup>rd</sup> Phase 4<sup>th</sup> Phase

Fig. 13 1<sup>st</sup> Field 2<sup>nd</sup> Field

20 1<sup>st</sup> Period 2<sup>nd</sup> Period 3<sup>rd</sup> Period 4<sup>th</sup> Period

$X(4p+1)-X(4p+2)^{th}$  (1<sup>st</sup> Phase)

$X(4p+2)-X(4p+3)^{th}$  (2<sup>nd</sup> Phase)

$X(4p+3)-X(4p+4)^{th}$  (3<sup>rd</sup> Phase)

$X(4p+4)-X(4p+5)^{th}$  (4<sup>th</sup> Phase)

25 Fig. 14

Fig. 15 Video Signal Converter Field Memory  
Control Signal Generator Circuit

Scan-sustain Driver A Scan-sustain Driver B

Address Driver A Address Driver B

30 Sustain Driver A Sustain Driver B

Fig. 16 Y Collector Circuit 1 Y Collector Circuit 2

Scan IC Scan IC Scan IC

X Collector Circuit 1 X Collector Circuit 2

X Collector Circuit 3 X Collector Circuit 4

35 Fig. 17 L1(Select) L5(Select) L9(Select)

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Fig. 28 Line Line

Reset Period Scanning Direction Address Period  
DisplayPeriod Blankingperiod ResetPeriod ScanningDirection  
Address Period Display Period  
Blanking period Reset Period Scanning Direction  
5 Address Period Display Period Blanking period(1) Reset Period  
Scanning Direction Address Period Display Period  
Reset Period Scanning Direction Address Period Display Period  
Fig. 29(a) Fig. 29(b) To A Electrode  
Fig. 30 YVoltageWaveform XCurrentWaveform YCurrentWaveform  
10 A Current Waveform A Voltage Waveform  
Fig. 31 YVoltageWaveform XCurrentWaveform YCurrentWaveform  
A Current Waveform A Voltage Waveform  
Fig. 32 Fig. 33 Yn Voltage Waveform 33 Yn+1 Voltage Waveform

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